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1 CLAIMS:

2 1. An integrated circuit device comprising:  
3 a semiconductor die;  
4 a first housing encapsulating the semiconductor die;  
5 a heat sink positioned proximate to the first housing; and  
6 a second housing encapsulating at least a portion of the heat  
7 sink.

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9 2. The integrated circuit device according to claim 1 further  
10 comprising at least one first lead coupled with the semiconductor die  
11 and the first housing encapsulates at least a portion of the at least one  
12 first lead.

13  
14 3. The integrated circuit device according to claim 1 wherein  
15 the heat sink comprises:

16 a body; and  
17 at least one second lead coupled with the body and the second  
18 housing encapsulates at least a portion of the at least one second lead.

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20 4. The integrated circuit device according to claim 3 wherein  
21 the at least one second lead is configured to dissipate heat from the  
22 semiconductor die.  
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1           5.    The integrated circuit device according to claim 1 wherein  
2 the second housing encapsulates a majority of the heat sink.

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4           6.    The integrated circuit device according to claim 1 wherein  
5 the second housing encapsulates a majority of the heat sink and at  
6 least a portion of the first housing.

7  
8           7.    The integrated circuit device according to claim 1 wherein  
9 the second housing encapsulates a majority of the heat sink and a  
10 majority of the first housing.

11  
12           8.    The integrated circuit device according to claim 1 wherein  
13 the semiconductor die comprises a synchronous-link dynamic random  
14 access memory device and the second housing forms one of a vertical  
15 surface mounted package and a horizontal surface mounted package.  
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1 9. An integrated circuit device comprising:  
2 a semiconductor die having a plurality of bond pads;  
3 a plurality of leads electrically coupled with the bond pads of the  
4 semiconductor die;  
5 a first housing encapsulating the semiconductor die and at least  
6 a portion of the leads;  
7 a heat sink thermally coupled with the first housing; and  
8 a second housing encapsulating at least a portion of the heat  
9 sink.

10  
11 10. The integrated circuit device according to claim 9 wherein  
12 the heat sink comprises a metal and the first housing contacts the  
13 metal.

14  
15 11. The integrated circuit device according to claim 9 wherein  
16 the heat sink includes at least one lead configured to dissipate heat  
17 from the semiconductor die.

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19 12. The integrated circuit device according to claim 9 wherein  
20 the second housing forms one of a vertical surface mounted package  
21 and a horizontal surface mounted package.

22  
23 13. The integrated circuit device according to claim 9 wherein  
24 the second housing encapsulates the first housing.

14. An integrated circuit device comprising:

a first housing formed about a semiconductor die and at least portions of a plurality of leads electrically coupled with the semiconductor die;

a heat sink thermally coupled with the first housing; and

a second housing formed about the heat sink and at least a portion of the first housing.

15. The integrated circuit device according to claim 14 wherein the first housing and second housing individually comprise an encapsulant housing.

16. The integrated circuit device according to claim 14 wherein the heat sink contacts the first housing.

17. The integrated circuit device according to claim 14 wherein the heat sink further includes at least one lead configured to dissipate heat from the semiconductor die.

18. A synchronous-link dynamic random access memory device comprising:

a semiconductor die bearing synchronous-link dynamic random access memory circuitry and having a plurality of bond pads coupled therewith;

a plurality of leads electrically coupled with the bond pads of the semiconductor die;

a first housing encapsulating the semiconductor die and at least a portion of the leads;

a heat sink positioned proximate the first housing and configured to draw heat from the semiconductor die; and

a second housing encapsulating the heat sink and at least a portion of the first housing.

19. The synchronous-link dynamic random access memory device according to claim 18 wherein the second housing forms one of a vertical surface mounted package and a horizontal surface mounted package.

20. The synchronous-link dynamic random access memory device according to claim 18 wherein the heat sink comprises at least one lead configured to dissipate heat from the semiconductor die.

1 21. A method of forming an integrated circuit device comprising:  
2 providing a semiconductor die;  
3 forming a first housing about the semiconductor die;  
4 thermally coupling a heat sink with the first housing; and  
5 forming a second housing about at least a portion of the heat  
6 sink following the thermally coupling.

7  
8 22. The method according to claim 21 wherein the providing  
9 comprises providing a semiconductor die coupled with plural leads of a  
10 lead frame.

11  
12 23. The method according to claim 22 further comprising  
13 bending the leads to form one of a vertical surface mounted package  
14 and a horizontal surface mounted package.

15  
16 24. The method according to claim 21 wherein the forming the  
17 first housing and the forming the second housing individually comprise  
18 encapsulating.

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20 25. The method according to claim 21 wherein the forming the  
21 second housing comprises encapsulating at least a portion of the first  
22 housing.  
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1 26. The method according to claim 21 further comprising  
2 providing the heat sink with at least one lead.  
3

4 27. A method of forming an integrated circuit device comprising:  
5 providing a semiconductor die having a plurality of bond pads;  
6 providing a first lead frame having a plurality of leads;  
7 providing a second lead frame having a heat sink;  
8 electrically coupling the bond pads of the semiconductor die with  
9 the leads of the first lead frame;

10 first encapsulating the semiconductor die and at least a portion  
11 of the leads, the first encapsulating forming a first housing;  
12 thermally coupling the heat sink with the first housing; and  
13 second encapsulating at least a portion of the heat sink forming  
14 a second housing following the thermally coupling.  
15

16 28. The method according to claim 27 wherein the second  
17 encapsulating further comprises encapsulating at least a portion of the  
18 first housing.  
19

20 29. The method according to claim 27 wherein the second  
21 encapsulating further comprises encapsulating a majority of the heat sink  
22 and a majority of the first housing.  
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1 30. The method according to claim 27 wherein the thermally  
2 coupling comprises positioning the heat sink to contact the first housing.

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4 31. The method according to claim 27 further comprising  
5 bending the leads to form one of a vertical surface mounted package  
6 and a horizontal surface mounted package.

7  
8 32. The method according to claim 27 wherein the providing the  
9 second lead frame comprises providing the heat sink with at least one  
10 lead.

11  
12 33. A method of forming an integrated circuit device comprising:  
13 providing a semiconductor die electrically coupled with a plurality  
14 of leads;

15 forming a first housing about the semiconductor die and at least  
16 a portion of the leads;

17 providing a heat sink; and

18 forming a second housing about at least a portion of the heat  
19 sink, the forming the second housing thermally coupling the heat sink  
20 with the semiconductor die.

21  
22 34. The method according to claim 33 further comprising  
23 positioning a heat sink proximate the first housing prior to forming the  
24 second housing.



1 35. The method according to claim 33 wherein the forming the  
2 first housing and the forming the second housing individually comprise  
3 encapsulating.

4  
5 36. The method according to claim 33 wherein the forming the  
6 second housing comprises forming the second housing about at least a  
7 portion of the first housing.

8  
9 37. The method according to claim 33 wherein the forming the  
10 second housing comprises encapsulating at least a portion of the heat  
11 sink and at least a portion of the first housing.

12  
13 38. The method according to claim 33 wherein the providing the  
14 heat sink comprises providing the heat sink having at least one lead.

15  
16 39. The method according to claim 33 further comprising  
17 bending the leads to form one of a vertical surface mounted package  
18 and a horizontal surface mounted package.

40. A method of forming a synchronous-link dynamic random access memory edge-mounted device comprising:

providing a semiconductor die having a plurality of bond pads;

providing a first lead frame having a plurality of leads;

providing a second lead frame having a heat sink;

electrically coupling the bond pads of the semiconductor die with the leads of the first lead frame;

positioning the semiconductor die and the first lead frame within a first mold following the electrically coupling;

first encapsulating the semiconductor die and at least a portion of the leads within the first mold using a first encapsulant;

curing the first encapsulant forming a first housing;

removing the first housing from the first lead frame;

positioning the heat sink of the second lead frame to contact a surface of the first housing;

providing the semiconductor die and the second lead frame within a second mold following the positioning the heat sink;

second encapsulating the first housing and the heat sink within the second mold using a second encapsulant;

curing the second encapsulant forming a second housing;

removing the second housing from the second lead frame;

trimming the leads; and

bending the leads to form one of a vertical surface mounted package and a horizontal surface mounted package.